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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,380	11/30/2004	Toshiki Makimoto	14321.63	2860

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EXAMINER	
NGUYEN, TRAM HOANG	
ART UNIT	PAPER NUMBER
2818	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/516,380	MAKIMOTO ET AL.	
	Examiner	Art Unit	
	TRAM H. NGUYEN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *50,51,53,56,77,78,80-82,85-89 and 96* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *50,51,53,56,77,78,80-82,85-89,96* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/22/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 50,51,53,56,77,78,80-82,85-89,96 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 50,51,53,56,77,78,80-82,85-89,96 are rejected under 35 U.S.C. 103(a) as being unpatentable over Makimoto (US 2002/0195619; hereinafter Makimoto), in view of Shiraishi (US 6,392,262), and further in view of K. Kumakura, T.

Makimoto and N. Kobayashi, Low-Resistance Nonalloyed Ohmic Contact to p-type GaN Using Strained InGaN Contact Layer, Applied Physics Letters, Vol. 79, No. 16, pp 2588-2590 (2001).

Regarding **claim 50**, Makimoto disclose a nitride semiconductor structure (fig. 10) comprising on a substrate (item 101):

an n-type collector layer (item 104);

a p-type base layer (refer to the lower half portion of 106) formed over said n-type collector layer (104), wherein said p-type base layer (106) is p-type InGaN;

an n-type emitter layer (107) formed directly on said p-type base layer (refer to the lower half portion of 106),

Makimoto fails to teach an indium-containing p-type nitride semiconductor layer formed directly on a second portion of said top surface of said p-type base layer, wherein said n-type emitter layer is not formed on the second portion, and said indium-containing p-type nitride semiconductor layer has an indium mole fraction that is higher than an indium mole fraction of said p-type InGaN base laver, and does not contact said n-type emitter layer.

Fig. 6 of Shiraishi discloses a similar nitride semiconductor structure (fig. 6) comprising on a substrate (item 1):

an n-type collector layer (item 10);

a p-type base layer (12) formed over said n-type collector layer (10), wherein said p-type base layer (12);

an n-type emitter layer (13) formed directly on said p-type base layer (refer to the upper center portion of 12);

an indium-containing p-type nitride semiconductor layer (6) formed directly on a second portion of said top surface of said p-type base layer (refer to the left or right portion of 12), wherein said n-type emitter layer is not formed on the second portion.

Thereof, it would have been obvious to one having ordinary skills in the art at the time the invention was made to combine the structure of Shiraishi in the teaching of Makimoto so that it results in a highly reliable and well reproducible hetero-junction bipolar transistor (see Shiraishi: col. 8, lines 8-14).

Makimoto and Shiraishi teach said p-type nitride semiconductor layer has an indium mole fraction higher than an indium mole fraction of said p-type InGaN base layer.

Kumakura exhibits that the contact resistance decreased with increase In mole fraction of p-type InGaN contact up to 0.19 (see p. 2589, col. 1, paragraph 1).

Thereof, it would have been obvious to one having ordinary skills in the art at the time the invention was made to combine the teaching of Kumrakura in the combined nitride semiconductor device structure of Makimoto and Shiraishi in order to reduce the contact resistance (see p. 2589, col. 1, paragraph 1).

The combination of Makimoto/ Shiraishi and Kumakura teaches said p-type nitride semiconductor layer (according to Kumakura, the InGaN layer having In mole fraction from 0.14-0.23 as recited in col.2, line 12) has an indium mole fraction higher

than an indium mole fraction of said p-type InGaN base layer (according to Makimoto, the indium mole fraction of p-InGaN base is 6% as shown in fig. 10).

Regarding **claim 51**, Makimoto/ Shiraishi and Kumakura disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides, Makimoto teaches said p-type nitride semiconductor layer (refer to the upper portion of p-type InGaN 106).

Regarding **claim 53**, Makimoto/ Shiraishi and Kumakura disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides, Makimoto teach said p-type InGaN base layer has an indium mole fraction of 5-30% (see fig. 10 exhibits the p-type InGaN base containing 6% of Indium).

Regarding **claim 56**, Makimoto/ Shiraishi and Kumakura disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides, Makimoto teach said p-type InGaN base layer has an indium mole fraction of 5-30% (see claim 53's rejection).

Regarding **claim 77**, Makimoto/ Shiraishi and Kumakura disclose all the limitations of the claimed invention for the same reasons as set forth above. Furthermore, Fig. 10 of Makimoto shows a graded layer (105) between the p-type base layer (106) and the n-type collection layer (item 104); wherein the graded layer (106) has its indium mole fraction varied gradually (see par.[0009],lines 1-3).

Regarding **claim 78**, Makimoto/ Shiraishi and Kumakura disclose all the limitations of the claimed invention for the same reasons as set forth above. Furthermore, Fig. 10 of Makimoto shows a graded layer (105) between the p-type base

layer (106) and the n-type collection layer (item 104); wherein the graded layer (105) has its indium mole fraction varied gradually (see par.[0009],lines 1-3).

Regarding **claim 80**, Makimoto/ Shiraishi and Kumakura disclose all the limitations of the claimed invention for the same reasons as set forth above. Besides, fig. 10 of Makimoto shows the base electrode (109) is formed directly on said indium-containing p-type nitride semiconductor (refer to the upper portion of 16).

Regarding **claim 81**, Makimoto discloses a nitride semiconductor structure (fig. 10) comprising:

an n-type collector layer (item 104);

a p-type base layer (refer to the lower half portion of 106) formed over said n-type collector layer (104), wherein the p-type base layer (refer to the lower half portion of 106) has an etched top surface (refer to the exposed portion of the lower portion 106) and is p-type InGaN (106);

an n-type emitter layer (107) formed directly on said p-type base layer (refer to the lower half portion 106).

Makimoto fails to teach an indium-containing p-type nitride semiconductor layer formed directly on a second portion of said top surface of said p-type base layer, wherein said n-type emitter layer is not formed on the second portion, and said indium-containing p-type nitride semiconductor layer has an indium mole fraction that is higher than an indium mole fraction of said p-type InGaN base laver, and does not contact said n-type emitter layer.

Fig. 6 of Shiraishi discloses a similar nitride semiconductor structure (fig. 6) comprising on a substrate (item 1):

an n-type collector layer (item 10);

a p-type base layer (12) formed over said n-type collector layer (10), wherein said p-type base layer (12);

an n-type emitter layer (13) formed directly on said p-type base layer (refer to the upper center portion of 12);

an indium-containing p-type nitride semiconductor layer (6) formed directly on a second portion of said top surface of said p-type base layer (refer to the left or right portion of 12), wherein said n-type emitter layer is not formed on the second portion.

Thereof, it would have been obvious to one having ordinary skills in the art at the time the invention was made to combine the structure of Shiraishi in the teaching of Makimoto so that it results in a highly reliable and well reproducible hetero-junction bipolar transistor (see Shiraishi: col. 8, lines 8-14).

Makimoto and Shiraishi teach said p-type nitride semiconductor layer has an indium mole fraction higher than an indium mole fraction of said p-type InGaN base layer.

Kumakura exhibits that the contact resistance decreased with increase In mole fraction of p-type InGaN contact up to 0.19 (see p. 2589, col. 1, paragraph 1).

Thereof, it would have been obvious to one having ordinary skills in the art at the time the invention was made to combine the teaching of Kumrakura in the combined

nitride semiconductor device structure of Makimoto and Shiraishi in order to reduce the contact resistance (see p. 2589, col. 1, paragraph 1).

The combination of Makimoto/ Shiraishi and Kumakura teaches said p-type nitride semiconductor layer (according to Kumakura, the InGaN layer having In mole fraction from 0.14-0.23 as recited in col.2, line 12) has an indium mole fraction higher than an indium mole fraction of said p-type InGaN base layer (according to Makimoto, the indium mole fraction of p-InGaN base is 6% as shown in fig. 10).

Regarding **claim 82**, Makimoto/ Shiraishi and Kumakura disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides, Makimoto teaches said indium-containing p-type nitride semiconductor layer (refer to the upper portion of 106) is p-type InGaN.

Regarding **claim 85,** Makimoto/ Shiraishi and Kumakura disclose all the limitations of the claimed invention for the same reasons as set-forth above. Furthermore, fig. 10 of Makimoto shows a graded layer (105) between said p-type base layer (refer to the lower portion of 106) and n-type collector layer (104).

Regarding **claim 86**, Makimoto/ Shiraishi and Kumakura disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides, Makimoto teaches the p-type nitride semiconductor layer (refer to the upper half portion of 106) has a thickness of between 1 and 1000nm (NOTE: fig. 10 exhibits that the thickness of 106 is 100nm; thereof, half of the thickness 106 is 50 nm).

Regarding **claim 87**, Makimoto/ Shiraishi and Kumakura disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides,

Makimoto teaches the p-type nitride semiconductor layer has a thickness of between 1 and 100nm NOTE: fig. 10 exhibits that the thickness of 106 is 100nm; thereof, half of the thickness 106 is 50 nm).

Regarding **claim 88**, Makimoto/ Shiraishi and Kumakura disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides, Makimoto teaches the p-type nitride semiconductor layer (refer to the upper portion of 106) has a thickness of between 1 and 1000nm (NOTE: fig. 10 exhibits that the thickness of 106 is 100nm; thereof, half of the thickness 106 is 50 nm).

Regarding **claim 89**, Makimoto/ Shiraishi and Kumakura disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides, Makimoto teaches the p-type nitride semiconductor layer (refer to the upper half portion of 106) has a thickness of between 1 and 100nm (NOTE: fig. 10 exhibits that the thickness of 106 is 100nm; thereof, half of the thickness 106 is 50 nm).

Regarding **claim 96**, Makimoto/ Shiraishi and Kumakura disclose all the limitations of the claimed invention for the same reasons as set forth above. Besides, fig. 6 of Shiraishi shows the base electrode (7) is formed directly on said indium-containing p-type nitride semiconductor layer (6).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tram Hoang Nguyen whose telephone number is (571) 272-5526. The examiner can normally be reached on 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (703)872-9306. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

THN
Art Unit 2818

/DAO H NGUYEN/
Primary Examiner, Art Unit 2818
May 26, 2009

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